**Computer science department, Langara college**

**Digital Systems Design (with FPGAs)**

**Spring 2019**

**Lab Delivery on Feb 11th**

**State machine delivery before the beginning of the lab**

# Lab 4: Finite State Machines (Sequence detector)

by S. Arash Sheikholeslam

In this lab, you will learn about state machines. In part 2 of the lab you will build a two branch state machine.

**Preparation:**

The following must be done before you come into the lab:

1. Read this handout before you start the lab.
2. Answer the state-machine questions on a separate paper before the lab. Treat it like an assignment
3. There is 4 points for the state machines. If your state machines are wrong, you will be given the correct one but will be marked out of 6

**Questions [4 points]**

**Plot two state machines diagrams for part 1 and part 2 of the lab.**

Part 1 [3 points]

For the first part you will make a circuit that can identify this pattern in sequences of length 5: 10001. In order to input the sequence, you will use **sw0** along with **key1,** key1 will act as your clock. Therefore, if you want to enter zero, you put sw0 to low and push the key1 once. If you want to enter two successive zeros you push the key1 twice.  
Conditions:  
1. We want the state machine to turn on **ledr0** once it recognized the sequence upon the last clock pulse. The next clock pulse should turn the led off.

2. If you input the following sequence 100010001 your ledr0 should only turn on at the 5th clock pulse.

Part 2 [3 points]

This is like part 1 except for now you have to identify two sequences: 10001 and 11000. If the circuit identified 10001 **ledr0** should turn on and if it identified 11000 then **ledr0** should turn on. Note that, you are dealing with a somewhat more complicated state machine here.

Conditions:

1.The above conditions still apply.

Example: if you input 001110001111, the ledr0 should turn on at the 8th pulse.

**Performance in the lab: (6 marks)**

In this lab, you will download the circuit you designed in the Preparation on the FPGA board. The input and output pins of this FPGA are tied to the various lights and switches.

1. Read the manual carefully

1. BE SURE that you set the pin assignments before compiling your design (not doing so could damage the board!). If you have any questions about how to do this, please talk to the TA.

You must demonstrate that your circuit works to the TA or to me by the end of your lab section.

*Marking:*

Your mark for the performance part of the lab will be:

0/6: If you don’t even show up, or if you show up and don’t do anything

1/6: If you make an attempt, but really don’t get anywhere near it working

4/6: If you almost get it working, or if you get it working but can’t answer TA’s questions.

6/6: If you successfully demonstrate your design to the TA, and can answer TA’s questions.